RISC-V

This document shows summary status about Phase 1 of project, which is simulating Dhrystone benchmark on nSIM simulator.

1. **Instructions**

Table 1 shows the needed instructions to run Dhrystone benchmark for risc-v which were obtained by simulating the benchmark on QEMU/Spike simulators. Basically, the support of each instruction will include 4 items: Decode, Disassemble, Execute and Test. The status can be shown through the color scheme as follows.

Done

In Progress

Table 1. Instruction Summary Status

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Item** | **instruction** | **Decode** | **Disassemble** | **Execute** | **Test** |
| **ALU** | | | | | |
|  | add |  |  |  |  |
|  | or |  |  |  |  |
|  | sll |  |  |  |  |
|  | sltu |  |  |  |  |
|  | srl |  |  |  |  |
|  | sub |  |  |  |  |
|  | addi |  |  |  |  |
|  | andi |  |  |  |  |
|  | ori |  |  |  |  |
|  | slli |  |  |  |  |
|  | sltiu |  |  |  |  |
|  | srai |  |  |  |  |
|  | srli |  |  |  |  |
|  | xori |  |  |  |  |
|  | mul |  |  |  |  |
|  | div |  |  |  |  |
|  | divu |  |  |  |  |
|  | remu |  |  |  |  |
| **Memory** | | | | | |
|  | lw |  |  |  |  |
|  | lbu |  |  |  |  |
|  | lhu |  |  |  |  |
|  | sw |  |  |  |  |
|  | sb |  |  |  |  |
|  | sh |  |  |  |  |
| **Control** | | | | | |
|  | blt |  |  |  |  |
|  | bltu |  |  |  |  |
|  | bge |  |  |  |  |
|  | bgeu |  |  |  |  |
|  | beq |  |  |  |  |
|  | bne |  |  |  |  |
|  | jal |  |  |  |  |
|  | j |  |  |  |  |
|  | jalr |  |  |  |  |
|  | jr |  |  |  |  |
|  | ret |  |  |  |  |
| **Control Status Registers** | | | | | |
|  | csrrs |  |  |  |  |
|  | csrr |  |  |  |  |
|  | csrs |  |  |  |  |
|  | csrrw |  |  |  |  |
|  | csrw |  |  |  |  |
| **Miscellaneous** | | | | | |
|  | auipc |  |  |  |  |
|  | lui |  |  |  |  |
|  | fence |  |  |  |  |
|  | li |  |  |  |  |
|  | mv |  |  |  |  |
|  | neg |  |  |  |  |
|  | seqz |  |  |  |  |
|  | bleu |  |  |  |  |
|  | beqz |  |  |  |  |
|  | bgt |  |  |  |  |
|  | bltz |  |  |  |  |
|  | bgez |  |  |  |  |
|  | bgtu |  |  |  |  |
|  | ble |  |  |  |  |
|  | bnez |  |  |  |  |
|  | blez |  |  |  |  |

1. **Registers**

The registers needed by Dhrystone benchmark are listed in Table 2, and the table will show its status.

Table 2. Registers Summary Status

|  |  |  |
| --- | --- | --- |
| **Item** | **Registers** | **Status** |
|  | mhartid |  |
|  | mstatus |  |
|  | mtvec |  |
|  | mcycle |  |
|  | minstret |  |

1. **Revision History**

Table 3. Review History

|  |  |  |
| --- | --- | --- |
| **Reviewer** | **Update Summary** | **Date** |
| Shaimaa Elsayed | First Version | 29/11/2022 |
| Mostafa Helmy | Couple of updates and restructure | 29/11/2022 |
| Mostafa Helmy | Marking ALU R-type Execute instructions as done.  Marking memory instructions (lw, sw) for decode, disasm, execute as done.  Marking multiply instructions as in progress for disasm. | 6/12/2022 |
| Mostafa Helmy | Mark decode and disasm of multiply insn as done.  Mark execute of multiply insn as in progress.  Mark disasm of alu immediate insn as done.  Mark decode and disasm of load insn variants as in progress. | 15/12/2022 |
| Mostafa Helmy | Mark test of alu register based insn as done.  Mark execute of load insn variants as in progress. |  |